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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANTS' REPLY BRIEF ON APPEAL

APPELLANT:	Tohisharu Yanagida	OLD DOCKET NO.:	P99,1318
		NEW DOCKET NO.:	09792909-4298
SERIAL NO.:	09/385,959	GROUP ART UNIT:	2822
DATE FILED:	August 30, 1999	EXAMINER:	D. Graybill
INVENTION:	"SEMICONDUCTOR APPARATUS AND PROCESS OF PRODUCTION THEREOF"		

Mail Stop Appeal Brief - Patents
Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Appellant submits herewith Appellants' Reply Brief on Appeal under 37 C.F.R. §41.41 in response to the Examiner's Answer mailed on July 7, 2006.

The Commissioner is hereby authorized to charge any deficiency in fees associated with this communication or credit any overpayment to Deposit Account No. 19-3140. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,


(Reg. No. 45,034)

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CERTIFICATE OF MAILING

I hereby certify that this original and two copies of this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 7, 2006.

(Reg. No. 45,034)
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Dear Sir:

In accordance with the provisions of 37 C.F.R. §41.41, Appellants submit this Reply Brief on Appeal in response to the Examiner's Answer mailed on July 7, 2006. Appellants respectfully submit that the Examiner's assertions are incorrect as a matter of fact and law. Thus, for the reasons set forth below, Appellants respectfully request that this Board reverse the rejections of claims 7, 8, and 10-21 under 35 U.S.C. §103.

I. STATUS OF CLAIMS:

Claims 1-8 and 10-21 are pending in the application. The present appeal is directed to claims 7, 8, and 10-21, which were finally rejected in an Office Action dated August 4, 2005. A copy of claims 7, 8, and 10-21 is appended to Appellants' Main Brief on Appeal as an Appendix.

The status of the claims on appeal is as follows:

Claims 7, 8, 10, 11, 16, and 19-21 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes (U.S. Patent No. 6,114,187)("Hayes")* in view of *Hotchkiss (U.S. Application No. 2002/0106832)("Hotchkiss")* and *Behun (U.S. Patent No. 5,147,084)("Behun")*.

Claims 12, 13, and 17 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes , Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al. ("U.S. Patent No. 6,227,436")("Nishikawa")* and *Denning, et al. ("U.S. Patent No. 6,187,682")("Denning")*.

Claims 14 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss, Behun, Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura ("U.S. Patent No. 4,807,021")("Okumura")*.

Claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes, Hotchkiss* and *Behun*, and further in view of *Jackson ("U.S. Patent No. 5,068,040")("Jackson")*.

II. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL:

A. Claims 7, 8, 10, 11, 16, and 19-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes (U.S. Patent No. 6,114,187)("Hayes")* in view of *Hotchkiss (U.S. Application No. 2002/0106832)("Hotchkiss")* and *Behun (U.S. Patent No. 5,147,084)("Behun")*.

B. Claims 12, 13, and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Nishikawa, et al. ("U.S. Patent No. 6,227,436")("Nishikawa")* and *Denning, et al. ("U.S. Patent No. 6,187,682")("Denning")*.

C. Claims 14 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss*, *Behun*, *Nishikawa et al.* and *Denning et al.*, and further in view of *Okumura ("U.S. Patent No. 4,807,021")("Okumura")*.

D. Claim 18 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Hayes*, *Hotchkiss* and *Behun*, and further in view of *Jackson ("U.S. Patent No. 5,068,040")("Jackson")*.

III. ARGUMENT:

Claims 7, 8, and 10-21 stand rejected under 35 U.S.C. §103 by the Examiner as being unpatentable based on various references. As set forth more clearly below, the rejections of the claims set forth by the Examiner under §103 are improper and accordingly the Board should reverse these rejections.

Each of the rejections includes a combination of references that includes *Hayes* in view of *Hotchkiss* and *Behun*, which the Examiner alleges discloses or suggests metal ball bumps formed in direct contact with a circuit pattern with eutectic solder layers formed on the surfaces of the metal ball bumps. As described below, *Hayes* in view of *Hotchkiss* and *Behun* fails to make such a teaching. Therefore, each of the rejections of the claims set forth by the Examiner under §103 are improper.

A. *Hayes* teaches away from using metal ball bumps formed in direct contact with a circuit pattern

The Examiner alleges that *Hayes* teaches using metal ball bumps formed in direct contact with a circuit pattern, however, *Hayes* actually teaches away from using metal ball bumps formed in direct contact with a circuit pattern. The Examiner cites *Hayes* 10:18-29, in which *Hayes* explains how to form solder columns by jetting drops of solder onto a substrate. In this passage, *Hayes* states that "[i]f the drops are very close together in time, they will solidify into one big ball of solder." *Hayes* 10:25-27. The Examiner has misinterpreted this to mean that individual solder balls are formed. Instead, the passage clearly describes that if drops are applied too quickly, a continuous "big ball of solder" will be formed instead of individual separate solder columns. In other words, the solder columns will run together, because the first solder drop will not solidify before the next solder drop is applied. This is clearly described in the surrounding text at *Hayes* 10:10-27 (emphasis added):

> In best mode a 63/37 tin/lead solder which melts at about 185.degree. C. is heated to about 220.degree. C. for jetting. A typical range is about 200-230.degree. C. with the substrate heated within a range of about 25.degree. to 150.degree. C. A typical substrate temperate is about 75.degree. C. The effect of temperature is somewhat complex because both the jetted droplet temperature and substrate affect the freezing process, as does the size and rate of the drops and the distance they travel after leaving the orifice in the printhead. Generally things that reduce the freezing rate tend to create a column that is wider and not as tall. If a longer time is provided between drops (normal operation is around 200 drops per second) the preceding drops have more time to freeze before the next drop arrives. This tends to build a narrower taller column. If the drop temperature is higher or there is less time between drops, the column tends to be fatter and lower. If the drops are very close together in time, they will solidify into one big ball of solder.

Thus, this passage from *Hayes* teaches that its solder columns can be narrow or wide depending on the processing conditions. It does not suggest using metal ball bumps, instead of solder columns, as alleged by the Examiner.

Further, Applicant correctly stated in the Main Brief on Appeal that *Hayes* 9:62-10:9 teaches away from forming metal ball bumps directly on a chip. *Examiner's Answer,* Page 13, lines 1-7. *Hayes* 9:62-10:9 clearly describes that it is especially valuable to form solder columns directly on chip pads instead of metal ball bumps, because metal ball bumps would contact each other (and cause physical or electrical interference) when the underlying pads are too close. Metal ball bumps are then formed on top of the solder columns. *Hayes* 9:67-10:1. The Examiner argues that *Hayes* 9:62-10:9 describes that interference is avoided between the metal balls that are formed *on top of* the solder columns, but this is not correct. The text in *Hayes* is quite clear: solder columns are formed on chip pads, and metal ball bumps are formed on the solder columns, thereby avoiding interference that would result between metal ball bumps had they been formed directly on the chip pads. *Hayes* 10:3-9.

Hayes also teaches that conventional approaches ("Ball Grid Arrays, Micro Ball Grid Arrays, Flip-Chip, and Chip Scale Packages") that used metal ball bumps were undesirable, because the conventional metal ball bumps were not formed directly on a chip and provided a larger than desired package. *Hayes* 1:60-62; 2:1-14. Accordingly, *Hayes* teaches forming solder columns directly on a chip, instead of metal ball bumps, in order to achieve a smaller package and to improve reliability. *Hayes* 2:30-35; 3:52-58 ("Very small packages can be created no bigger than the integrated chip itself. There is a certain amount of flexibility added to the electrical connections by the solder columns, which improves reliability.") Thus, in these additional passages, *Hayes* also teaches away from forming metal ball bumps directly on a chip.

B. It would not have been obvious to substitute the metal ball bumps of *Hotchkiss* for the solder columns of *Hayes*

As described above, *Hayes* teaches away from metal ball bumps formed in direct contact with a circuit pattern. *Hayes* forms solder columns 3 on its circuit pads 2 and then forms solder balls 9 on top of its solder columns, in order to achieve a smaller package and to improve reliability. *Hayes* 2:30-35; 3:52-58 ("Very small packages can be created no bigger than the integrated chip itself. There is a certain amount of flexibility added to the electrical connections by the solder columns, which improves reliability.") Therefore, contrary to the Examiner's argument, it would not have been obvious to substitute the metal ball bumps of *Hotchkiss* for the solder columns of *Hayes*. *Examiner's Answer,* page 12, lines 18-20.

C. *Behun* also discloses metal ball bumps formed on solder columns, not metal ball bumps formed in direct contact with a circuit pattern

Like *Hayes, Behun* teaches forming metal ball bumps 18 on LMP solder 16 (*i.e.* LMP solder columns). *See, Behun* Figure 1. Thus, like *Hayes, Behun* also fails to disclose forming metal ball bumps in direct contact with a circuit pattern.

Therefore, none of the cited references, taken individually or in combination, teaches eutectic solder layers formed on metal ball bumps that are formed in direct contact with a circuit pattern.

Appellants respectfully request that the Board reverse the rejection.

IV. CONCLUSION:

For the foregoing reasons, Appellants respectfully submit that the rejections posed by the Examiner are improper as a matter of law and fact. Accordingly, Appellants respectfully request the Board reverse the rejections of claims 7, 8, and 10-21.

Respectfully submitted,

(Reg. No. 45,034)

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